Product Brief

LSI™ StarPro2704 (SP2704) Multicore Media and Baseband Processor

Multicore Done Right™

FEATURES

- **Four StarCore® SC3400e DSP subsystems at 750 MHz:**
  - – Enhanced instruction set for voice, video, and cellular baseband applications
  - – 16 MAC DSP engines
  - – 256-KB local RAM
  - – 32-KB L1 instruction cache
  - – 32-KB L1 data cache
  - – 512-KB L2 cache
  - – Two dedicated 2-channel DMA controllers
- **Dual-core ARM11 MP™ RISC processors at 375MHz:**
  - – 64-KB instruction cache per core
  - – 64-KB data cache per core
  - – 512-KB local memory
- **Ultrahigh bandwidth DSP bus matrix as a system interconnect for the media processing functional blocks:**
  - – 128-bit, multilayer ARM® AXI™ buses that operate at half the DSP subsystem clock rate
  - – High throughput with high availability and low latency
- **Hardware assist for wireline speed IP/UDP or proprietary head processing (verify and classify):**
  - – IPV6 supported
- **6-MB shared system memory with error detection and correction:**
  - – Unified memory space provide both instruction and data store
  - – Banked implementation maximizes throughput and minimize contention
  - – Twelve banks allow for 12 simultaneous transactions
- **Error correction coding (ECC) on all memories except ARM core memories that support parity detection**
- **Two 10/100/1000/2500-Mb/s Ethernet MACs:**
  - – Supports 4-wire SGMII interfaces
  - – IEEE® 802.3u compliant
  - – Supports MDIO interface
  - – 1000BASE-KX compliant
- **TDM processing block supports six serial ports for multiplexing and demultiplexing TDM traffic:**
  - – Direct interface to H.110 and ST-BUS (1X or 2X compatible) compliant devices, T1/E1 framers, and more than one concentration highway interface (CHI) on many LSI devices
  - – Support for up to 256 time slots per TDM highway
  - – Maximum input clock rate of 124.8 MHz and output bit clock rate of 62.4 MHz
  - – Two dedicated DMA channels (one input, one output) that support each serial port
- **Two 2-channel DMACs for efficiency in moving data among the memory and peripherals**
- **Coprocessor connectivity ports for high-speed direct access to other SP2704 devices or coprocessors, or alternate function as host interface port:**
  - – 10-Gb/s x2 PCIe® Gen 2 interface (two 5 Gb/s lanes)
  - – 10-Gb/s x4 sRIO interface (four 3.125-Gb/s lanes) or alternative configuration as two independent x1 SRIO interfaces
  - – PCIe Gen 2 interface (two 5-Gb/s lanes)
- **32-bit DDR3 external memory interface accessible by the DMA controllers and processors**
- **Two IEEE 1149.1-compliant JTAG ports for on-chip emulation of the CPU and DSP subsystems**
- **21 mm x 21 mm package with 0.8-mm ball pitch**

Overview

The SP2704 media and baseband processor is the third generation of LSI multicore DSP and RISC CPU platforms based on StarCore DSPs. Representing the latest media and baseband processor in the multicore processor portfolio from LSI, the SP2704 targets a wide range of next-generation wireless, wireline, and enterprise infrastructure applications with high channel density, optimal cost, and power efficiencies.

This heterogeneous computing platform is optimized for low-power and high density applications, enabling very high channel densities for media and basestation applications.

The SP2704 is complemented by the LSI Media Processing Suite, a comprehensive software library optimized for high density, multi-channel applications. The library includes wireless and wireline audio codecs, video codecs, echo cancellers and other voice quality enhancement (VQE) modules, IP packet processing, and a flexible and highly efficient media processing engine.

A packet processing subsystem, based ARM11 MP processors, performs the processing and routing of IP packets, providing many system control plane options. Complementing the large shared system memory, full support for external memory is provided using DDR3 memory controller. A robust peripheral set includes PCIExpress®, Serial Rapid I/O (sRIO), TDM, and Ethernet interfaces. The DSP subsystems, ARM subsystem, system memory, and I/O are connected through a high-performance bus matrix based on a multilayer ARM AXI host bus. This bus matrix is effectively a crossbar switch, providing more than 144-GB/s of aggregate throughput.

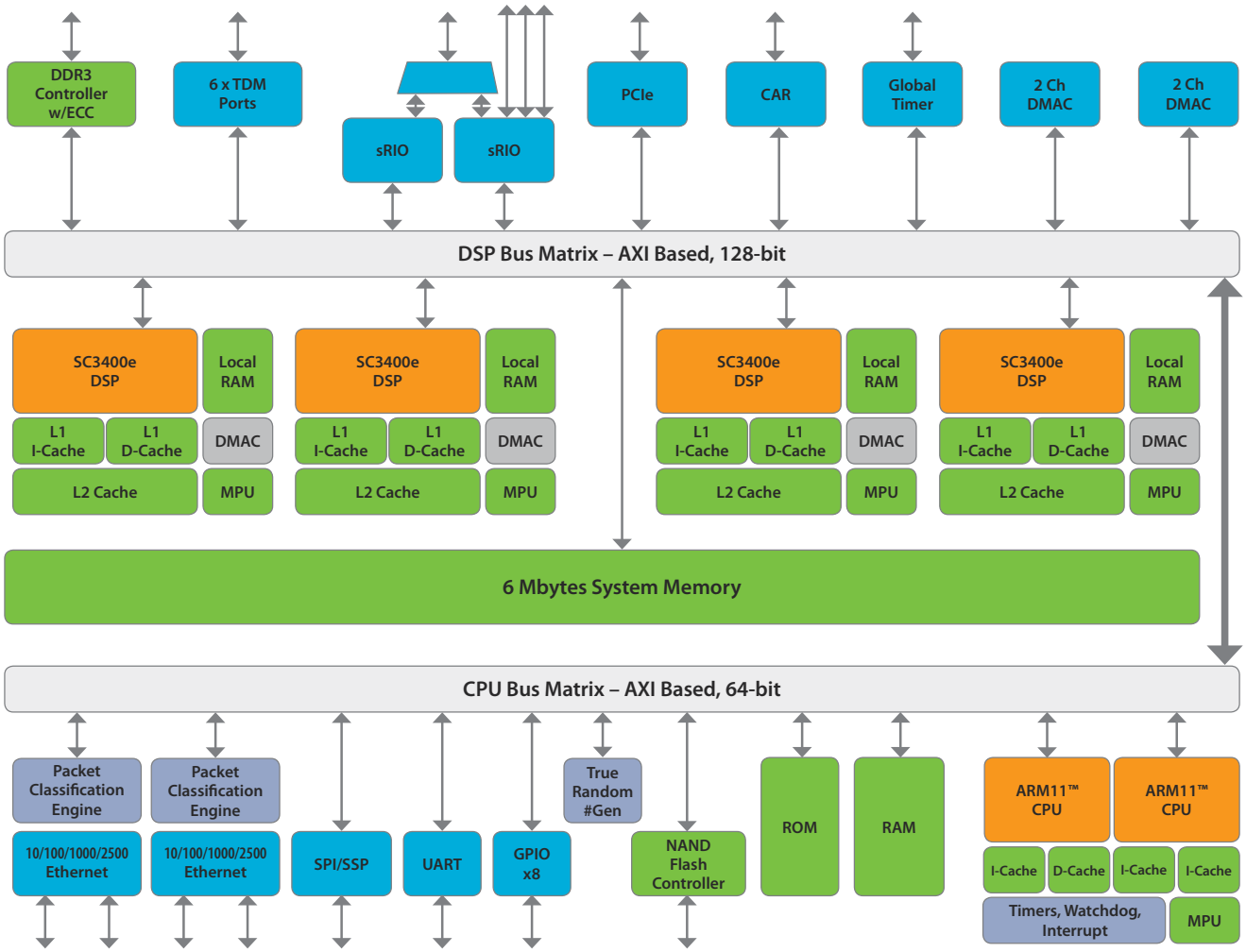

Figure 1 SP2704 Media & Baseband Processor Block Diagram

Typical channel capacities:

- G.711 to TDM: 800
- G.729A/B to TDM: 456
- AMR to TDM: 364

Ordering Information: ADN: L-SP27041FP750-DB Comcode: 711022960

For more information and sales office locations, please visit the LSI web sites at: lsi.com

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